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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/736,724	12/13/2000	Shunpei Yamazaki	07977-175002	8339

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EXAMINER

BROCK II, PAUL E

ART UNIT	PAPER NUMBER
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2815

DATE MAILED: 03/31/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/736,724	Applicant(s) YAMAZAKI ET AL.	
	Examiner Paul E Brock II	Art Unit 2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 27 October 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-23, 25-29, 31-36, 38-43, 45-57 and 59-74 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 3-23, 25-29, 31-36, 38-43, 45-57, 59-67 and 69-73 is/are allowed.
- 6) ☒ Claim(s) 1, 2, 68 and 74 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 13 December 2000 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☒ Certified copies of the priority documents have been received in Application No. 08/912,979.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>20031027</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1, 2, 68, and 74 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mase et al. (USPAT 6236064, Mase) in view of Mukai et al. (USPAT 5585658, Mukai) and Zhang et al. (USPAT 5403772, Zhang).

With regard to claim 1, it is inherent in the method of Mase that in order to implant ions into only parts of the channel formation region a mask has to be formed over a crystal semiconductor comprising a part to become a channel forming region. Further it is inherent in the method of Mase that a dotted hole would have to be formed in the mask. Mase discloses in figures 5a – 5c and column 5, lines 27 – 40 forming a substantially intrinsic region and impurity regions in the part to become the channel forming region by introducing a first impurity into the channel forming region having the dotted hole, the first impurity being oxygen. Mase also discloses in figures 5a – 5c and column 5, lines 27 – 40 introducing into the crystal semiconductor a second impurity that gives one conductivity to form a source region and a drain region in the crystal semiconductor with the channel forming region therebetween. It is inherent in the method of Mase that the impurity regions are formed through a mask over a crystal

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semiconductor. Mase does not disclose that the impurity region is formed through a resist mask with a dotted pattern that is patterned by the focused ion beam (FIB) method. Mukai discloses in figures 3a – 3e forming a resist mask (16) and patterning (17) the resist mask by using FIB method (18). It would have been obvious to one of ordinary skill in the art to use the resist and patterning using the FIB method of Mukai in the method of Mase in order to optimally control an impurity profile as discussed by Mukai in column 1, lines 54 – 58. Mase and Mukai do not teach the substantially intrinsic region has an oxygen concentration below 2×10^{18} atoms/cm³. Zhang teaches in column 9, lines 67 – 68 and column 10, lines 1 – 7 a substantially intrinsic region having an oxygen concentration less than 10^{18} atoms/cm³. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the concentration of impurity of Zhang in the method of Mase and Mukai in order to obtain a higher mobility as stated by Zhang in column 9, lines 67 – 68 and column 10, lines 1 – 7. Mase discloses in column 5, lines 27 – 40 that the impurity region occupies only parts of the channel formation region. Mase, Mukai, and Zhang do not disclose what percentage of the width of the channel region is occupied by the impurity region. It is well known in the art to have impurity regions that have a total width of W_{pi} in a direction of a width W , and a total of the intervals in W_{pa} in a direction of the width, wherein $W_{pi}/W = 0.1$ to 0.9 and $W_{pa}/W = 0.1$ to 0.9 . It would have been obvious to one of ordinary skill in the art at the time of the present invention to use percentage of the channel regions occupied by the impurity region of 10% to 90% in the method of Mase, Mukai, and Zhang in order to only occupy parts of the channel region so as to increase the carrier mobility of the charier region as stated by Mase in column 5, lines 27 – 40. Mase and Mukai are both silent to the transistor being used in a DRAM circuit, SRAM circuit, memory section, or

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arithmetic operating section. Zhang teaches in column 1, lines 7 – 24 many different types of circuits and semiconductor sections wherein a transistor may be provided including a DRAM circuit. All of the transistors disclosed by the references are TFTs. Therefore, it would have been further obvious to one of ordinary skill in the art at the time of the present invention wherein the source region and the drain region and the channel forming region of Mase, Mukai, and Zhang are provided in a transistor of a DRAM circuit in order to make use of the transistor as a TFT in a known semiconductor circuit.

With regard to claim 2, Mase discloses in figures 5a – 5c forming a gate insulating film over the part to become the channel forming region after the step of forming the plurality of impurity regions. Mase discloses in figures 5a – 5c forming a gate electrode over the part to become the channel forming region with the gate insulating film therebetween.

With regard to claim 68, Mase discloses in column 4, lines 55 – 64, and column 5, lines 27 – 40 wherein the substantially intrinsic region contains boron, and concentration of boron therein is 5×10^{15} , and the substantially intrinsic regions contains oxygen, and concentration of oxygen therein is 1×10^{18} .

With regard to claim 74, it is inherent in the method of Mase that in order to implant ions into only parts of the channel formation region a mask has to be formed over a crystal semiconductor comprising a part to become a channel forming region. Further it is inherent in the method of Mase that a dotted hole would have to be formed in the mask. Mase discloses in figures 5a – 5c and column 5, lines 27 – 40 forming a substantially intrinsic region and impurity regions in the part to become the channel forming region by introducing a first impurity into the channel forming region having the dotted hole, the first impurity being oxygen. Mase also

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discloses in figures 5a – 5c and column 5, lines 27 – 40 introducing into the crystal semiconductor a second impurity that gives one conductivity to form a source region and a drain region in the crystal semiconductor with the channel forming region there between. It is inherent in the method of Mase that the impurity regions are formed through a mask over a crystal semiconductor. Mase does not disclose that the impurity region is formed through a resist mask with a dotted pattern that is patterned by the focused ion beam (FIB) method. Mukai discloses in figures 3a – 3e forming a resist mask (16) and patterning (17) the resist mask by using FIB method (18). It would have been obvious to one of ordinary skill in the art to use the resist and patterning using the FIB method of Mukai in the method of Mase in order to optimally control an impurity profile as discussed by Mukai in column 1, lines 54 – 58. Mase and Mukai do not teach the substantially intrinsic region has an oxygen concentration below 2×10^{18} atoms/cm³. Zhang teaches in column 9, lines 67 – 68 and column 10, lines 1 – 7 a substantially intrinsic region having an oxygen concentration less than 10^{18} atoms/cm³. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the concentration of impurity of Zhang in the method of Mase and Mukai in order to obtain a higher mobility as stated by Zhang in column 9, lines 67 – 68 and column 10, lines 1 – 7. Mase discloses in column 5, lines 27 – 40 that the impurity region occupies only parts of the channel formation region. Mase, Mukai, and Zhang do not disclose what percentage of the width of the channel region is occupied by the impurity region. It is well known in the art to have impurity regions that have a total width of W_{pi} in a direction of a width W , and a total of the intervals in W_{pa} in a direction of the width, wherein $W_{pi}/W = 0.1$ to 0.9 and $W_{pa}/W = 0.1$ to 0.9 . It would have been obvious to one of ordinary skill in the art at the time of the present invention to use percentage of the

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channel regions occupied by the impurity region of 10% to 90% in the method of Mase, Mukai, and Zhang in order to only occupy parts of the channel region so as to increase the carrier mobility of the charier region as stated by Mase in column 5, lines 27 – 40.

Allowable Subject Matter

3. Claims 3 – 23, 25 – 29, 31 – 36, 38 – 43, 45 – 57, 59 – 67, and 69 – 73 are allowed.

Response to Arguments

4. Applicant's arguments filed October 27, 2003 have been fully considered but they are not persuasive.

5. With regard to applicant's arguments that "the source region, and the drain region are provided not in a pixel section, as in Mase, but rather in a transistor of at least one selected from the group consisting of an arithmetic operating section, a memory section, a DRAM circuit and an SRAM circuit," it should be noted that Mase does not limit the invention from only being used in a pixel section. None of the references specifically state that the transistor cannot be used in one of the claimed arithmetic operating section, a memory section, a DRAM circuit and an SRAM circuit. Therefore, applicant's arguments are not persuasive, and the rejection is proper.

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6. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E Brock II whose telephone number is (571) 272-2723. The examiner can normally be reached on 8:30 AM - 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1164. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul E Brock II

A handwritten signature in black ink, appearing to read 'Paul E Brock II', with a long horizontal flourish extending to the right.